

REMARKS

Claims 14-26 are pending in the application. The claims have not been amended by the present amendment, and therefore stand as provided in the Preliminary Amendment filed with the application on March 23, 2001.

In response to the drawing objections, replacement sheets are provided, in which text labels have been added to the blocks in FIG. 1. In FIG. 2, the word "address" has been corrected. No new matter is added. Approval of the corrected drawings is respectfully requested.

Applicants appreciate the information about the guidelines for preferred layout of the specification. This application was filed originally in the German Patent Office in the German language, and claims priority therefrom. Applicants submit a substitute specification under 37 CFR 1.125(b) including relevant subheadings. No new matter is added. Also enclosed is a marked-up comparison of the original English translation of the specification and the Substitute Specification.

Applicants' claimed invention is directed to an apparatus and method for picture-in-picture insertion, wherein a sequence of insertion pictures decimated by vertical decimation are read into a memory device and subsequently read out, and wherein the insertion pictures read out are inserted into a sequence of main pictures. As recited in claims 14 and 22, the memory device for storing the insertion pictures has a storage capacity of less than two insertion pictures and is subdivided into memory segments, where more than one memory segment is required for storing an insertion picture.

For example, as shown in FIGS. 2a-2c, the memory device has a storage capacity of 1.5 fields and is subdivided into three memory segments X, Y, and Z (each having a storage capacity of 0.5 field), which are continuously overwritten as shown in FIGS. 2a-2c. According to the Applicants' claimed invention, reduced cost can be achieved by using a smaller memory device, while still preventing the read pointer from overtaking the write pointer during picture-in-picture insertion (see substitute specification at page 2, lines 2-15).

Claims 14-26 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 5,369,442 to Braun. This rejection is respectfully traversed.

Braun fails to teach or suggest a method or circuit arrangement for picture-in-picture insertion having a memory device with a storage capacity of less than two insertion pictures, and in which more than one memory segment of the memory device is required for storing an insertion picture.

Referring to column 6, lines 33-65 and FIG. 2, as cited in the Office Action, Braun discloses a first video source Q1 providing a sequence of main pictures H₁, H₂, and a second video source Q2 providing a sequence of insertion pictures K₁, K₂, where each insertion picture is inserted into one main picture. In Braun, the insertion pictures K₁, K₂ are referred to as "half-frames," where each half-frame is transmitted at a 50 Hz or 60 Hz television frequency (see column 6, lines 13-23 of Braun). The "half-frames" K₁, K₂ in Braun are entire pictures, and thus correspond to the insertion pictures of the Applicants' invention. *then you don't have an invention*

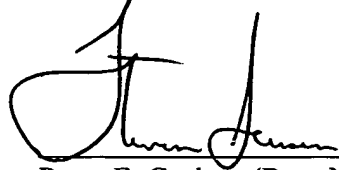
In Braun, a memory device SP has two memory regions SP1, SP2 for storing the insertion pictures K₁, K₂, respectively, where each memory region stores one insertion picture (see column 6, lines 46-54).

In contrast to the Applicants' claimed invention, the memory device SP in Braun does **not** have a storage capacity of less than two insertion pictures, but instead has a storage capacity equal to two insertion pictures. Moreover, the memory device SP is not subdivided into memory segments having a capacity of less than one insertion picture, as required in claims 14 and 22. In Braun, the memory device SP is subdivided into two memory segments SP1, SP2, each memory segment having the capacity for storing one insertion picture.

For at least the reasons described above, Braun fails to anticipate or otherwise render obvious the Applicants' claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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~~Description~~ TITLE: METHOD AND CIRCUIT ARRANGEMENT FOR PICTURE-
IN-PICTURE INSERTION

~~Method and circuit arrangement for picture-in-picture~~
5 ~~insertion~~

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a method for picture-in-picture insertion ~~in~~
10 ~~accordance with the preamble of claim 1, and to a circuit arrangement~~
~~for picture-in-picture insertion in accordance with the preamble of~~
~~claim 9.~~

2. Description of Related Art

15 In the case of such picture-in-picture (PIP) insertion ~~(PIP)~~, a smaller
insertion picture (small picture) is inserted into a larger main picture. The insertion
picture is decimated in accordance with the size reduction and is continuously read into a
memory device, older stored pictures being overwritten, and then the insertion pictures
are read out in a manner employing synchronization with the main pictures. Accordingly,
20 the read-out speed of the insertion pictures is generally higher than the writing speed. In
this case, the main picture and the insertion picture may, in a known manner, be fields
which are used for displaying a monitor picture.

At specific phase angles of the rasters of the main picture and of the small picture,
the higher read-out speed can lead, inter alia, to the read-out pointer overtaking the write
25 pointer and reading out a previous picture stored in the memory device, with the result
that a seam occurs in the middle of a displayed small picture and in part the preceding
insertion picture is read out. If both insertion pictures originate from different motion
phases, a disturbing effect results since moving objects through which the seam runs are
displayed with distortion. If the frequencies of the pictures of the insertion channel and
30 main channel correspond only approximately, the result is slow drifting of the disturbance
location, which is found to be particularly unpleasant.

EP 0 739 130 A2 describes a method for eliminating this seam by storing two fields of a small picture, with the result that the field that can be read is always exactly the one which is currently not being written, and, consequently, the read pointer cannot overtake the write pointer. A first and a second memory, which each store a field, are provided for this purpose. This method has the disadvantage, however, that a storage capacity of two insertion pictures or fields is necessary, which entails corresponding costs.

BRIEF SUMMARY OF THE INVENTION

10 Accordingly, the invention is based on the object of providing a method and a circuit arrangement for picture-in-picture insertion with which the occurrence of a seam in the insertion picture can be prevented in a cost-effective manner and with a relatively low outlay on apparatus.

15 ~~This object is achieved by means of a method according to claim 1 and a circuit arrangement according to claim 9. The sub-claims describe preferred developments of the method according to the invention and of the circuit arrangement according to the invention.~~

20 The invention is based on the concept that it is not necessary, in principle, to store two whole insertion pictures in order to prevent the write pointer from being overtaken by the read pointer. Instead of using a storage capacity of two insertion pictures, a smaller memory device is subdivided into a suitable number of segments, and suitable decision-making is effected to stipulate whether the currently written or the preceding insertion picture is read out.

25 Consequently, according to the invention—, in contrast to the use of two separate memory segments for the currently written and the preceding insertion picture—, if appropriate even the currently written insertion picture is read out if it is ensured that the read pointer does not overtake the write pointer.

30 For this purpose, memory segments which, in particular, are the same size can be cyclically overwritten in a predetermined order since, in particular, good periodicity of the operation can also be ensured by this means. ~~The method according to the invention can be achieved in an advantageous manner by means of the dimensionings according to claims 3 to 6, in which~~

~~case, in particular, the decision criterion may be chosen according to claim 6.~~

BRIEF DESCRIPTION OF THE DRAWINGS

5 The invention is explained in more detail below using a number of embodiments with reference to the accompanying drawings in which:
Figure FIG. 1 ~~shows is~~ a block diagram of a circuit arrangement according to the invention;
Figure ~~2~~ ~~shows an illustration~~ FIGS. 2a, 2b, and 2c are illustrations of a
10 memory device according to a first embodiment of the invention; and
Figure FIG. 3 ~~shows is~~ an illustration of a memory device according to a second embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

15 In accordance with Figure FIG. 1, a sequence of main pictures $H_i = H_1, H_2, H_3, \dots$ are output from a main picture source 1 via a main picture channel 7 to a control device 3. Correspondingly, from an insertion picture source 2, a sequence of insertion pictures $K_j = K_1, K_2, K_3, \dots$ decimated by a decimation device 12, i.e. reduced in size relative to the main pictures, are output to a memory device S and buffer-stored.
20 In this case, both the main pictures H_i and the insertion pictures K_j are fields which are combined e.g. in a line-offset manner to form the overall monitor picture. Afterward, the sequence of small pictures is read out and forwarded to the control device 3 via an insertion picture channel 8. If an asynchronous main picture source 1 and insertion picture source 2 are used, the read-out operation of the memory device S is effected in a
25 manner exhibiting synchronization with the main pictures H_i . On account of the decimation, in particular the vertical decimation, the read-out of the insertion pictures K_j from the memory device by the control device 3 takes place more rapidly than the operation of writing to the memory device. The control device 3 combines the main pictures H_i and insertion pictures K_j to form an overall picture which is reproduced on a
30 monitor 6.

One-quarter (1/4) picture-in-picture insertion is assumed below, where the small picture is correspondingly decimated in each case by the factor 2 in the horizontal and

vertical. According to the invention, it is provided for this purpose that the memory device has a storage capacity of 1.5 fields (decimated relative to the main pictures) and, in accordance with ~~Figure 2~~, FIGS. 2a, 2b, and 2c, is subdivided into three memory segments X, Y and Z, all three segments being the same size, i.e. each having a storage capacity of 0.5 field (decimated relative to the main pictures) and being continuously overwritten in this cyclic order. Consequently, a writing start segment I and a second writing segment II are in each case required for a field.

Accordingly, in a first storage operation in accordance with ~~Figure~~ FIG. 2 a, a memory area formed from the start writing segment X and the second writing segment Y is written to ~~for~~ the first field K1. The second field K2 is correspondingly written to the start writing segment Z and the second writing segment X in the subsequent storage operation in accordance with ~~Figure~~ FIG. 2 b, the start segment of the first field K1 already being overwritten in the process of writing to the second writing segment X. During the third storage operation, the field K3 is correspondingly written to the start writing segment Y and the second writing segment Z in accordance with ~~Figure~~ FIG. 2 c. Consequently, at the instant when, in ~~Figure~~ FIG. 2 c, the write pointer is located in the start segment Y, in the location designated by SZ1, the second half of the first field K1 is overwritten, i.e., at this instant, K1 is still partly present, K2 is completely present and K3 is currently being written to the segment Y.

For the read-out operation it must be ensured that, on the one hand, a whole field is read out and, on the other hand, the read pointer does not overtake the write pointer. For this purpose, a decision must be made as to whether the currently written field K_j or the immediately preceding field K_{j-1} is read out. Since the difference in the writing and read-out speed is essentially determined by the vertical decimation VD, where VD is a natural number, the decision as to which field is to be read out can be made dependent in each case on VD and on the position of the write pointer in the currently written field. This position of the write pointer generally depends on the position of the small picture in the main picture and hence primarily on the phase angle of the small picture and main picture, the read pointer generally being fixedly coupled to the main picture via the insertion position.

In the case of a vertical decimation of VD=2, the read-out speed is about twice as high as the writing speed, with the result that the read pointer would overtake the write

pointer in the currently written field if the write pointer has only written less than half of the field, i.e. is still located in the start segment, as is the case in the position SZ1 in ~~Figure~~FIG. 2 c during the writing of the field K3. Consequently, the preceding field K2 must be read out in this case, i.e. the reading start segment is the writing start segment I of the previous field, i.e. the segment Z according to ~~Figure 2~~FIG. 2b. By contrast, at the position SZ2 in ~~Figure~~FIG. 2 c, at which the write pointer is already located in the second writing segment Z, the writing start segment Y can be taken as the reading start segment.

Generally, it can be derived from these considerations that $2*VD-1$ segments, each having a storage capacity which corresponds to the quotient of the storage capacity required for an insertion picture and VD, are necessary in order to ensure in each case that either the currently written or the immediately preceding insertion picture can be read out. The total memory space required is thus $(2-1/VD)$ times the storage capacity required for an insertion picture. The saving in comparison with the use of two memory areas for a respective insertion picture thus falls with increasing vertical decimation VD. Since the quotient of reading speed and writing speed can, to a good approximation, be applied as VD, the decisive criterion for the selection of the reading start segment is whether the last segment required for writing the current insertion picture is already being written to.

In the case of 1/9 picture-in-picture insertion, $VD=3$ and, in accordance with ~~Figure~~FIG. 3, it is necessary correspondingly to choose $2*VD-1=5$ segments A, B, C, D and E each having a storage capacity of $1/3$ field, with the result that a total storage capacity of $5/3$ fields is required. In this case, too, memory segments I, II, III are cyclically overwritten, with the result that the first field is written to the segments A, B and C, the second field to the segments D, E and A, etc. Since the reading speed is about three times higher than the writing speed, the decision criterion to be applied here is whether more than $1/VD = 1/3$ of the memory space required for a field remains to be written to. Consequently, in this case, too, the resulting decision criterion is whether the last segment—, in this case the third segment III—, required for the current field is already being written to.

In addition to the elimination of the seam, it is furthermore possible to eliminate disturbances that may arise as a result of different field positions in the insertion channel 8 and main channel 7, e.g., in the case of a picture composed of line-offset fields,

disturbances between the upper field in the main channel 7 and the lower field in the insertion channel 8. This can be ensured e.g. by storing an additional line, with the result that the lines of the upper field of the insertion channel, despite the dependence on the raster position of the field of the main channel, are always displayed relatively above the

5 lines of the lower field of the insertion channel.